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60 GHz Receiver (Rx) Waveguide Module

TECHNICAL DATA SHEET PEM002

The PEM002 is a highly integrated millimeter wave receiver that covers the 60 GHz global unlicensed spectrum allocations packaged in a standard waveguide module. Receiver architecture is a double conversion, sliding IF with wide bandwidth capability through the conversion chain down to baseband. The I/Q analog interface along with built-in AM and FM detectors provides for flexibility in design and applications. The receiver incorporates a complete waveguide interface with low-loss transition between the chip and the WR15 waveguide port. The integrated package is small and lightweight, with a simple to use multi-pin ST4 connector for power, reference clock, digital control port and baseband signals. Either of two reference clocks can be used for setting 540 MHz or 500 MHz channel spacing.

Features:

- Complete millimeter wave receiver
- WR-15, UG-385/U flange
- Operates in the 57 to 66 GHz unlicensed band
- 6 dB noise figure
- Up to 1.8 GHz modulation bandwidth
- I/Q analog baseband interface
- Integrated AM/ASK and FM/FSK detectors
- On chip synthesizer covers 57 to 64.8 GHz
- 500 MHz or 540 MHz step size
- 285.714 MHz clock for 500 MHz step size
- 308.572 MHz clock for 540 MHz step size
- Power, control, signals on ST4 connector
- Temperature sensor

Applications

- 802.11ad: 58.32, 60.48, 62.64, 64.80 GHz
- 802.11aj: 59.94, 61.02, 62.10, 63.18 GHz
- Any Channel (500 MHz or 540 MHz) 57-64.8 GHz
- Multi-Gbps Digital Communications
- HD Video Transmission
- Millimeter Wave Radar
- Millimeter Wave Radiometry
- Millimeter Wave Imaging
- Microwave Temperature Profiling (MTP)
- Development for 802.11ad and 802.11aj
- ATE Equipment for 60 GHz Manufacturing Test

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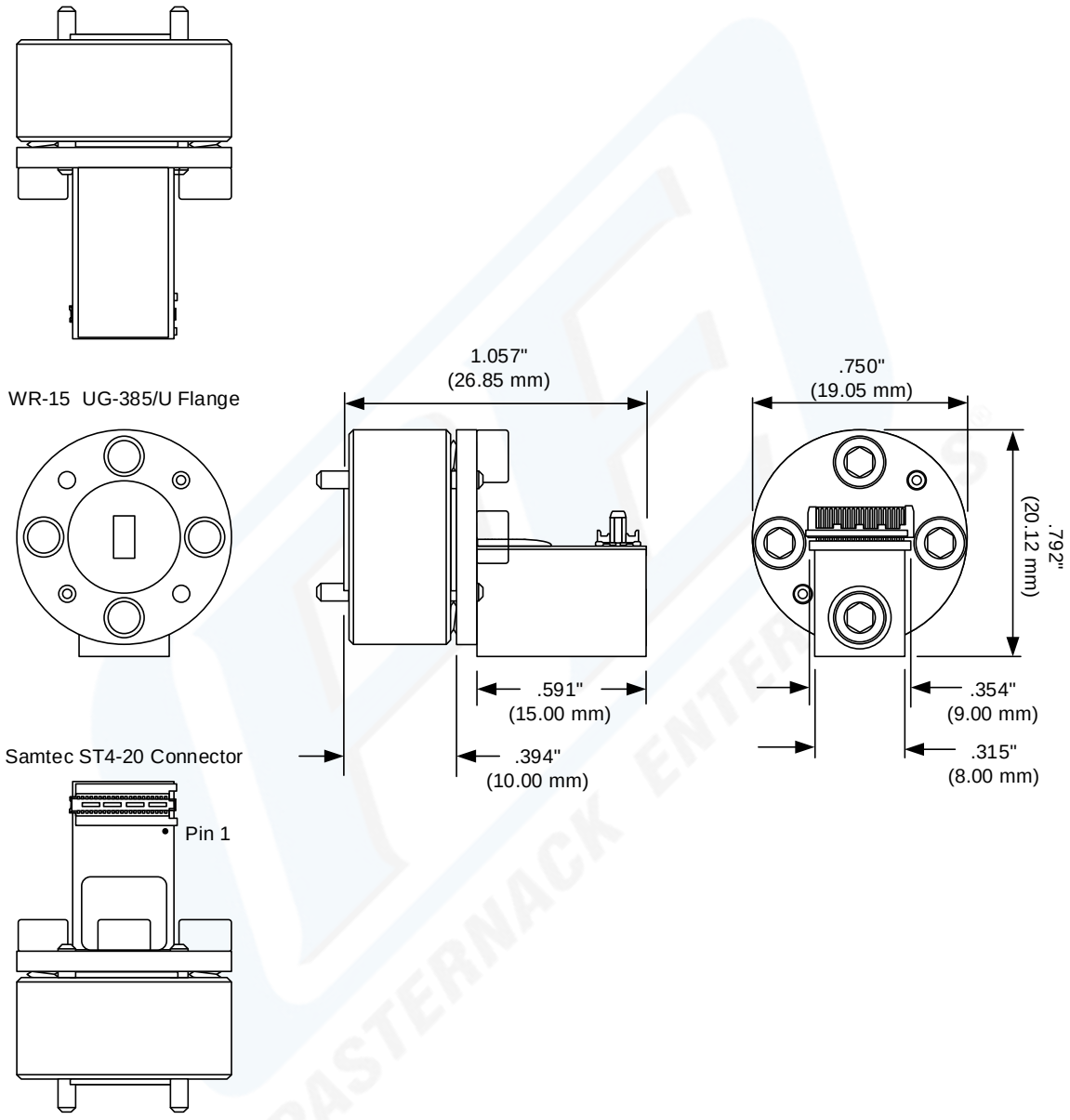

Figure 1 PEM002 Mechanical Dimensions

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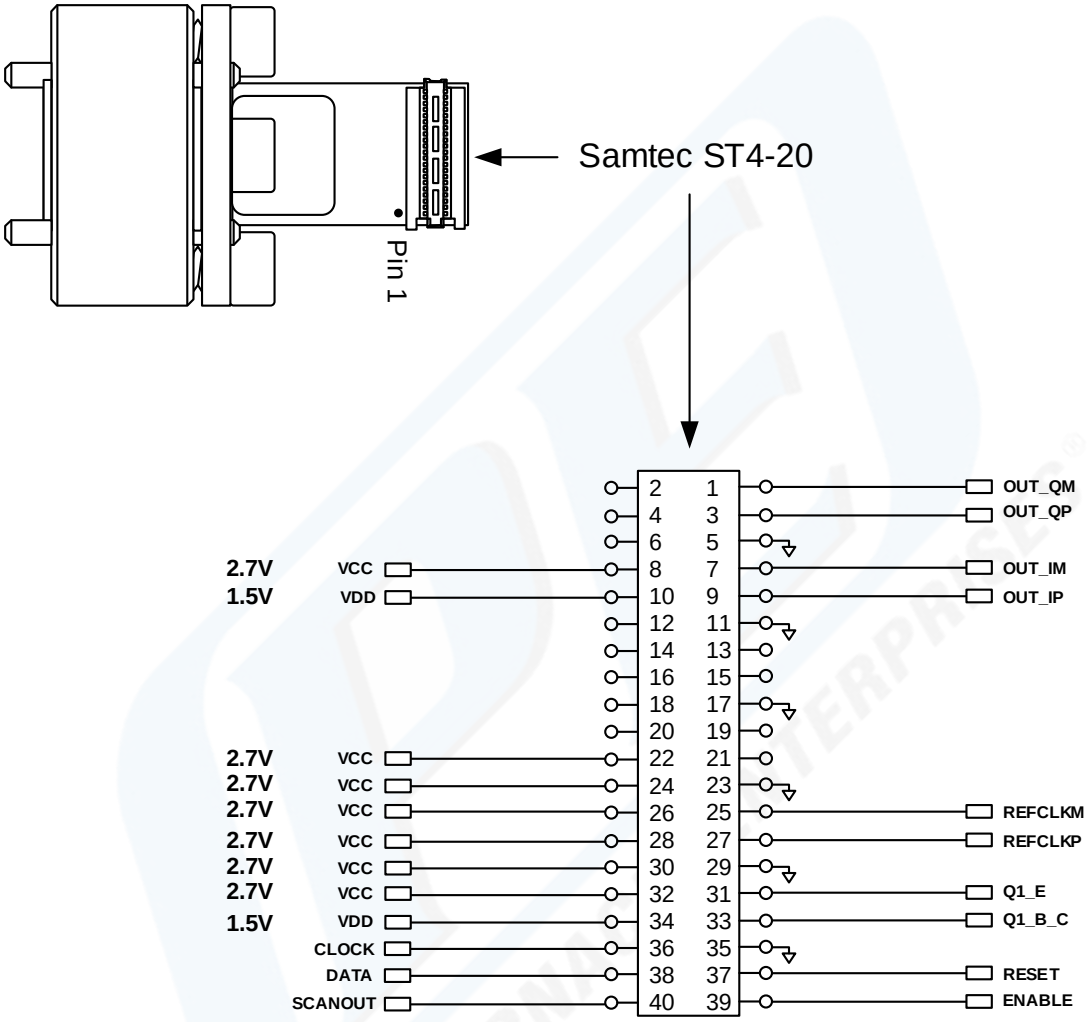

Mating Connector:
Samtec SS4-20-3.00-L-D-K-TR

Figure 2 PEM002 Interface Connector Pinout

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Table 1 Performance Specifications*

Parameter	Min	Typ	Max	Unit	Comment
Frequency Range	57.0		64.8	GHz	
Channel Spacing		540		MHz	308.571 MHz Reference
Channel Spacing		500		MHz	285.714 MHz Reference
Modulation Bandwidth		1.8		GHz	Max BW setting, double-sided at 3 dB
Gain, Max	53	67	70	dB	
Gain, Range		65		dB	
Gain, Step Size		1.25		dB	
Image Rejection		>35		dB	
Input IP3		-27		dBm	At Max Gain
Input P1dB		-36		dBm	At Min Gain
Sideband Suppression		27		dBc	
Noise Figure		6		dB	At Max Gain
Phase Noise @ 100 kHz		-72		dBc/Hz	
Phase Noise @ 1 MHz		-86		dBc/Hz	
Phase Noise @ 10 MHz		-111		dBc/Hz	
Phase Noise @ 100 MHz		-125		dBc/Hz	
Phase Noise @ 1 GHz		-127		dBc/Hz	
PLL Loop Bandwidth		200		kHz	
I/Q Balance Phase		± 3		degrees	
I/Q Balance Amplitude		± 1		dB	

*Test Conditions:

Reference Frequency	308.571 MHz
Temperature	25°C
Input Signal Level	-65 dBm
IF Bandwidth	Max
Output Impedance	50 ohms, 4 output ports: I +/- and Q +/- (100 ohm differential)
Output Signal Level	Referenced to single 50 ohm output for gain specifications

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Table 2 Recommended Operating Conditions

Description	Name	ST4 Pin #	Min	Typ	Max	Unit
Power Supplies	Vcc	8,22,24,26, 28,30,32	2.565	2.7	2.835	V
	Vdd	10,34	1.425	1.5	1.575	V
Serial Control Port Logic High	DATA	38	1.0	1.3	1.575	V
	CLOCK	36				
	ENABLE	39				
	RESET	37				
	SCANOUT	40				
Serial Control Port Logic Low	DATA	38	-.05	0.1	0.33	V
	CLOCK	36				
	ENABLE	39				
	RESET	37				
	SCANOUT	40				
Serial Control Port Speed					100	MHz
Reference Clock[1]	REFCLKM	25	-5	0	3	dBm
	REFCLKP	27				
I and Q Baseband[2]	OUT_QM	1	10	100	400	mVPP
	OUT_QP	3				
	OUT_IM	7				
	OUT_QP	9				
Temperature Sensor[3]	Q1_E	31				
	Q1_B_C	33				
Vcc 2.7V Supply Current	Icc			225		mA
Vdd 1.5V Supply Current	Idd			8		mA
Operating Temperature	T_A		-40		85	°C

[1] Reference clock power level specified at 100 ohms differential
[2] Baseband voltage at each of the 4 baseband outputs (I +/-, Q +/-)
[3] Temperature sensor is a 2N3904 NPN transistor die connected as a diode junction

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Table 3 Absolute Maximum Ratings

Description	Name	ST4 Pin #	MAX
Power Supplies	Vcc	8,22,24,26, 28,30,32	2.85 V
	Vdd	10,34	1.6 V
Serial Control Port Logic High	DATA	38	1.575
	CLOCK	36	
	ENABLE	39	
	RESET[1]	37	
	SCANOUT	40	
Serial Control Port Logic Low	DATA	38	-.05
	CLOCK	36	
	ENABLE	39	
	RESET[1]	37	
	SCANOUT	40	
Reference Clock	REFCLKM	25	5 dBm
	REFCLKP	27	
I and Q Baseband	OUT_QM	1	750 mVPP
	OUT_QP	3	
	OUT_IM	7	
	OUT_QP	9	
GND		5,11,17,23,29,35	± 50 mV
Power Dissipation	P_D		760 mW
Storage Temperature	T_S		-55 to 150 C
Operating Temperature	T_A		-40 to 85 C

[1] Assertion of RESET, active high, asynchronously resets all registers

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TECHNICAL DATA SHEET PEM002

Receiver Architecture

The PEM002 receiver uses a double conversion superheterodyne architecture with a sliding IF. The IF frequency is at 1/7 the RF carrier frequency, and the VCO is at 2/7 the RF carrier frequency. The LO is 3x the VCO frequency. The LO and IF are generated from a built-in synthesizer that has a step size at the RF carrier frequency of either 500 MHz or 540 MHz depending upon which reference clock frequency is used. The 540 MHz step size uses a 308.571 MHz reference, and the 500 MHz step uses a 285.714 MHz frequency. The IEEE channels for 802.11ad and 802.11aj are supported when the 540 MHz step size is used. An RF signal in the range of 57 to 64.8 GHz is coupled to the LNA via the low-loss WR15 waveguide port. The LO is mixed with the RF signal after the LNA and down converted the IF signal in the 8 to 9 GHz range. A notch filter attenuates the image frequency. The IF signal is filtered with a variable gain amplifier and filter with approximately 20 dB range, which is then fed into the quadrature mixers which down converts directly to baseband. There are also selectable AM and FM detectors for non-coherent modulation schemes. Additional variable gain and filtering are available in the baseband amplifier section which follows the I/Q mixers and detectors. The overall phase noise and I/Q balance specifications are sufficient for up to 16 QAM operation. Configuration and settings are controlled through a digital serial interface port. The block diagram below shows the various stages and circuits in the module.

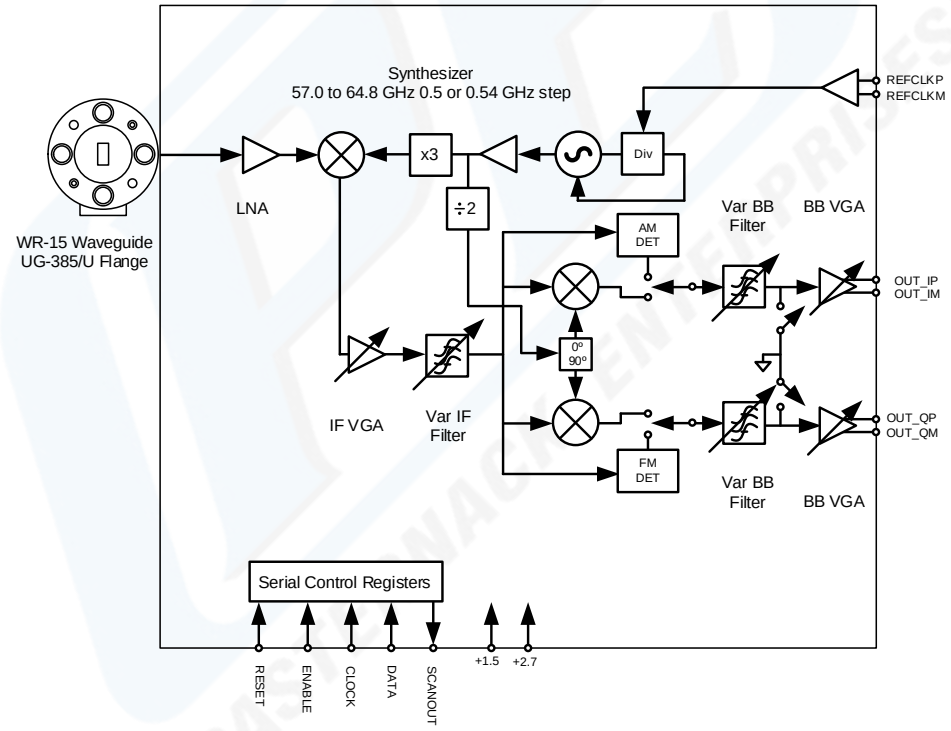

Figure 3 PEM002 Block Diagram

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60 GHz Receiver (Rx) Waveguide Module

Synthesizer Design

The PEM002 receiver uses a double conversion superheterodyne architecture with a sliding IF. The IF frequency is at 1/7 the RF carrier frequency, and the VCO is at 2/7 the RF carrier frequency. The LO is 3x the VCO frequency.

The tables below show the RF carrier, IF, VCO and LO for the frequency range from 57 GHz to 64.80 GHz at 540 MHz and 500 MHz channel spacing respectively. The reference clock for the synthesizer at 540 MHz spacing is 308.571 MHz; for 500 MHz spacing it is 285.714 MHz. The loop bandwidth of the synthesizer phase lock loop is 200 kHz.

540 MHz Spacing

f_{RF}	IF	VCO	LO
57.24	8.177	16.354	49.063
57.78	8.254	16.509	49.526
58.32	8.331	16.663	49.989
58.86	8.409	16.817	50.451
59.40	8.486	16.971	50.914
59.94	8.563	17.126	51.377
60.48	8.640	17.280	51.840
61.02	8.717	17.434	52.303
61.56	8.794	17.589	52.766
62.10	8.871	17.743	53.229
62.64	8.949	17.897	53.691
63.18	9.026	18.051	54.154
63.72	9.103	18.206	54.617
64.26	9.180	18.360	55.080
64.80	9.257	18.514	55.543

500 MHz Spacing

f_{RF}	IF	VCO	LO
57.00	8.143	16.286	48.857
57.50	8.214	16.429	49.286
58.00	8.286	16.571	49.714
58.50	8.357	16.714	50.143
59.00	8.429	16.857	50.571
59.50	8.500	17.000	51.000
60.00	8.571	17.413	51.429
60.50	8.643	17.286	51.587
61.00	8.714	17.429	52.286
61.50	8.786	17.571	52.714
62.00	8.857	17.714	53.143
62.50	8.929	18.587	53.571
63.00	9.000	18.000	54.000
63.50	9.071	18.143	54.429
64.00	9.143	18.286	54.857

Figure 4 Synthesizer RF, IF, VCO and LO Frequencies

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Digital Control Registers and Serial Interface Protocol - Write Operation

The PEM002 is configured via the serial control port which transfers data synchronously to or from (write or read operation) a register location. Register locations are organized into 16, byte-wide (8-bit) locations. The register locations are written to or read from one byte at a time as shown in Figures 5 and 6 respectively. Figure 5 shows the sequence of the digital control signals for the ENABLE, CLOCK and DATA input pins (ST4 connector, pins 39, 36 and 38 respectively) to write a single byte into the control register. After the ENABLE signal goes low, the first of 18 data bits (bit 0) is placed on the data pin, and 2 ns or more after the DATA signal stabilizes, the CLOCK signal goes high which clocks in data bit 0. The DATA signal must remain stable for at least 2 ns after the rising edge of the CLOCK. The signal levels are 1.5V CMOS, 50 kΩ impedance, with a maximum clock rate of 100 MHz.

A write operation requires an 18 bit field associated with 18 clock pulses as shown in Figure 5. The 18 bit field contains the 8-bit data (LSB is clocked in first), followed by the byte address (BYTE 0 through BYTE 15, 000000 to 001111, LSB first, only 4 of the 6 bits are used with the two MSBs set to 0), the read/write (R/W) bit (write = 1), and the module address which distinguishes between a transmitter module and receiver module (for the PEM002 receiver, RX module = 111).

After clock pulse 17 (18 total pulses), the ENABLE signal is returned to a high state to load the register byte into the module. The CLOCK signal must be stable in the low state at least 2 ns prior to the rising edge of the ENABLE signal.

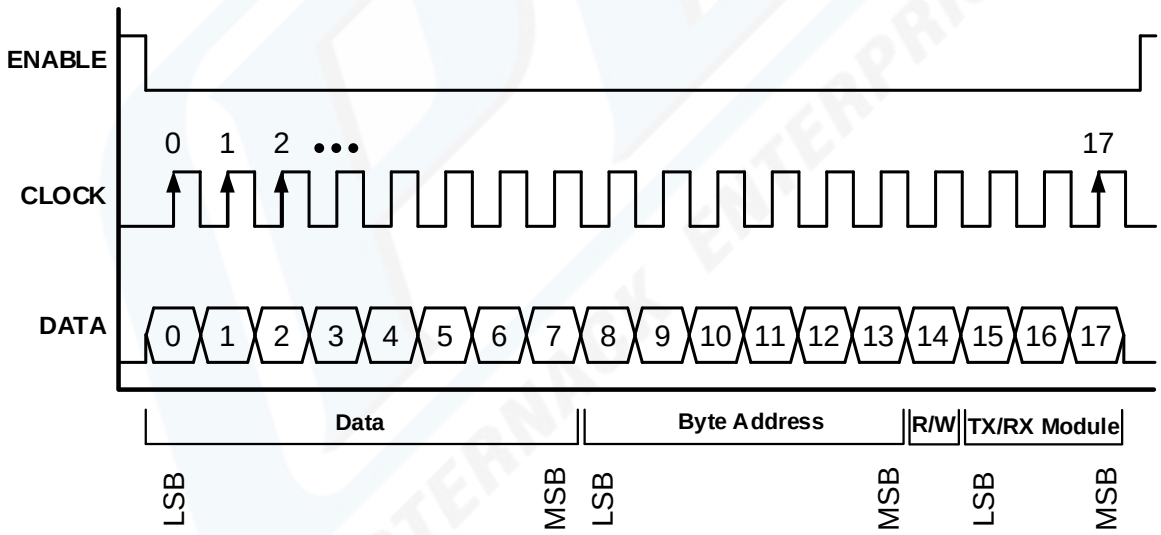

Figure 5 Write Operation Timing Diagram

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Digital Control Registers and Serial Interface Protocol - Read Operation

Figure 6 shows the sequence of control signals at the ENABLE, CLOCK and DATA pins to read a single byte at a register location. A read operation requires a 27 bit field: The first 18 bits are used to clock in the bits on the DATA input pin. The first 8 bits during a read operation are “don’t care” bits as they are placeholders for the 8-bit byte data which would be present during a write operation. The following 10 bits are composed of the byte address (BYTE 0 through BYTE 15, 000000 to 001111, LSB first, only 4 of the 6 bits are used with the two MSBs set to 0), the read/write (R/W) bit (read = 0), and the module address which distinguishes between a transmitter module and receiver module (for the PEM002 receiver, RX module = 111).

After clock pulse 17 (18 total pulses), the ENABLE signal is returned to a high state while the clock signal is low, then a single clock pulse (pulse 18) is sent during the ENABLE signal high period. The ENABLE signal then returns to the low state while the CLOCK signal is low. At each of the subsequent 8 CLOCK pulses, the 8-bit data from the specified register location is available at the SCANOUT pin, LSB first. Note that the DATA signal must remain in the low state during the period from clock pulse 18 through 26. Following clock pulse 26, the ENABLE signal goes high while the CLOCK signal is low to end the read operation.

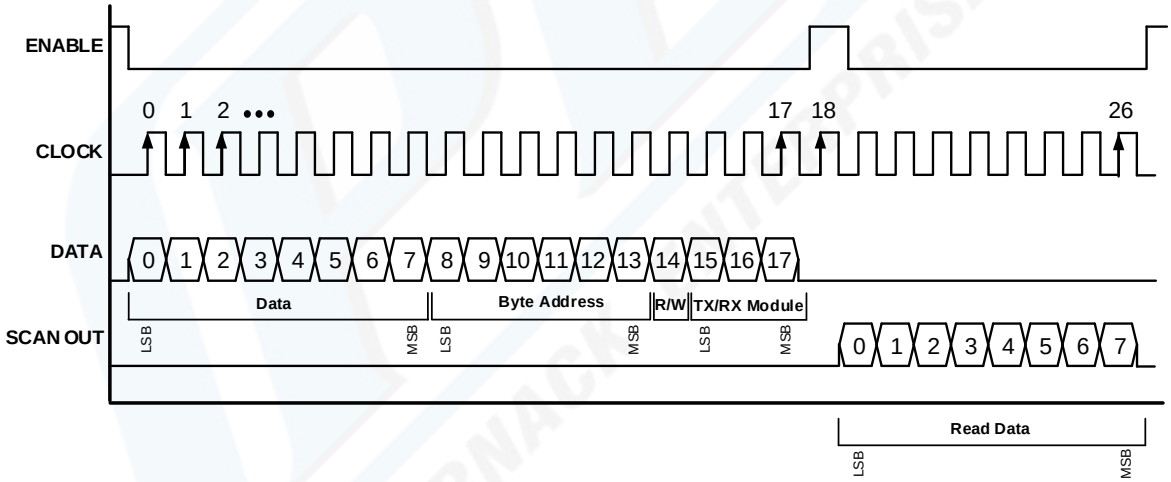

Figure 6 Read Operation Timing Diagram

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Table 4.1 Register Byte Functions

Bit	Name	Function
BYTE 0		
7	ask_pwrdn	Active high to power down ASK demodulator
6	bbamp_pwrdn_i	Active high to power down I-channel baseband amplifier
5	bbamp_pwrdn_q	Active high to power down Q-channel baseband amplifier
4	divider_pwrdn	Active high to power down local oscillator divider
3	if_bgmux_pwrdn	Active high to power down one of three on-chip refs (IF) and associated mux
2	ifmix_pwrdn_i	Active high to power down I-channel IF to baseband mixer
1	ifmix_pwrdn_q	Active high to power down Q-channel IF to baseband mixer
0	ifvga_pwrdn	Active high to power down IF variable gain amplifier
BYTE 1		
7	ipc_pwrdn	Active high to power down module current reference generator
6	lna_pwrdn	Active high to power down low noise amplifier and reference
5	rfmix_pwrdn	Active high to power down RF to IF mixer
4	tripler_pwrdn	Active high to power down frequency tripler
3	bbamp_atten1_0	First baseband attenuator: bits <2:3>
2	bbamp_atten1_1	11 = 18 dB; 10 = 12 dB; 01 = 6 dB; 00 = 0 dB
1	bbamp_atten2_0	Second baseband attenuator: bits <0:1>
0	bbamp_atten2_1	11 = 18 dB; 10 = 12 dB; 01 = 6 dB; 00 = 0 dB
BYTE 2		
7	bbamp_attenfi_0	I Channel baseband fine attenuator: bits <5:7>
6	bbamp_attenfi_1	101 = 5 dB; 100 = 4 dB; 011 = 3 dB; 010 = 2 dB; 001 = 1 dB; 000 = 0 dB
5	bbamp_attenfi_2	
4	bbamp_attenfq_0	Q Channel baseband fine attenuator: bits <2:4>
3	bbamp_attenfq_1	101 = 5 dB; 100 = 4 dB; 011 = 3 dB; 010 = 2 dB; 001 = 1 dB; 000 = 0 dB
2	bbamp_attenfq_2	
1	bbamp_selask	Active high to switch the ASK detector into the I channel baseband amplifier
0	bbamp_sigshort	Active high to short the inputs to the I and Q channel baseband amplifiers

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Table 4.2 Register Byte Functions

Bit	Name	Function
BYTE 3		
7	bbamp_selbw_0	Baseband amplifiers low pass filter corner: bits <6:7>
6	bbamp_selbw_1	00 = 1.4 GHz; 01 = 500 MHz ; 11 = 300 MHz; 00 = 200 MHz
5	bbamp_selhp_0	Baseband amplifiers high pass filter corner: bits <4:5>
4	bbamp_selhp_1	00 = 30 kHz; 01 = 300 kHz ; 10 = 1.5 MHz
3	bg_monitor_sel_1	Reserved: bits <3:0> = 0011 for normal operation
2	bg_monitor_sel_0	
1	lf_refsel	
0	lna_refsel	
BYTE 4		
7	ifvga_bias_2	IF VGA bias and IF filter alignment; bits <7:0> = 1001111x for normal operation
6	ifvga_bias_1	
5	ifvga_bias_0	
4	ifvga_tune_4	
3	ifvga_tune_3	
2	ifvga_tune_2	
1	ifvga_tune_1	
0	not used	
BYTE 5		
7	ifvga_vga_adj_3	IF VGA gain control bits; bits <7:4> = 0000 highest gain, 1111 lowest gain Attenuation 1.25 dB/step, ≈ 20 dB maximum
6	ifvga_vga_adj_2	
5	ifvga_vga_adj_1	
4	ifvga_vga_adj_0	
3	rfmix_tune_3	IF filter alignment in the RF mixer; bits <3:0> = 1111 for normal operation
2	rfmix_tune_2	
1	rfmix_tune_1	
0	rfmix_tune_0	

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Table 4.3 Register Byte Functions

Bit	Name	Function
BYTE 6		
7	tripler_bias_13	Frequency tripler bias (upper 8 bit portion): bits <7:0> = 10111111 default
6	tripler_bias_12	
5	tripler_bias_11	
4	tripler_bias_10	
3	tripler_bias_9	
2	tripler_bias_8	
1	tripler_bias_7	
0	tripler_bias_6	
BYTE 7		
7	tripler_bias_5	Frequency tripler bias (lower 6 bit portion): bits <7:2> = 011011 default
6	tripler_bias_4	
5	tripler_bias_3	
4	tripler_bias_2	
3	tripler_bias_1	
2	tripler_bias_0	
1	bbamp_sel_fm	Active high to switch the FM detector into the Q channel baseband amplifier
0	fm_pwrdn	Active high to power down FM detector
BYTE 8		
7	lna_bias_2	IF VGA gain control bits; bits <7:4> = 0000 highest gain, 1111 lowest gain
6	lna_bias_1	
5	lna_bias_0	
4	not used	Not used; bits <4:3> = xx
3	not used	
2	ifvga_q_cntrl_2	IF filter Q in the VGA amplifier; bits <2:0> = 000 for highest Q and gain For reduced Q and wider bandwidth, bits <2:0> = 001,100,101,111 in sequence
1	ifvga_q_cntrl_1	
0	ifvga_q_cntrl_0	

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Table 4.4 Register Byte Functions

Bit	Name	Function
BYTE 9		
7	not used	Not used: bits <7:0> = xxxxxxxx
6	not used	
5	not used	
4	not used	
3	not used	
2	not used	
1	not used	
0	not used	
BYTE 10		
7	rdacin_5	VCO amplitude DAC; bits<7:2> = 111100 for normal operation
6	rdacin_4	
5	rdacin_3	
4	rdacin_2	
3	rdacin_1	
2	rdacin_0	
1	synreset	Synthesizer reset; bit <1> = 0 for normal operation
0	divratio_4	Synthesizer divider ratio bit 4 (see Tables 5.1 and 5.2)
BYTE 11		
7	divratio_3	Synthesizer divider ratio bits 3:0 (see Tables 5.1 and 5.2)
6	divratio_2	
5	divratio_1	
4	divratio_0	
3	band_2	VCO band tuning bits 2:0 (see Tables 5.1 and 5.2)
2	band_1	
1	band_0	
0	rfseldiv	Reserved; bit <0> = 1 for normal operation

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Table 4.5 Register Byte Functions

Bit	Name	Function
BYTE 12		
7	cpbias_2	Synthesizer charge pump bias; bits <7:5> = 010 for normal operation
6	cpbias_1	
5	cpbias_0	
4	vrsel_3	Synthesizer lock detector window width; bits <4:1> = 1111 for normal operation
3	vrsel_2	
2	vrsel_1	
1	vrsel_0	
0	refselvco	Reserved; bit <0> = 1 for normal operation
BYTE 13		
7	muxref	Reserved; bit <7> = 1 for normal operation
6	div_4	Enable synthesizer divider bit 4; bit <6> = 0 for normal operation
5	en_dc	Synthesizer reference input DC coupling; bit <5> = 0 for normal operation
4	ini	Reserved; bit <4> = 0 for normal operation
3	pd_div_15	Active high to power down 1.5V circuits in synthesizer divider
2	pd_div_27	Active high to power down 2.7V circuits in synthesizer divider
1	pd_qp	Active high to power down synthesizer charge pump
0	pd_vco	Active high to power down synthesizer VCO
BYTE 14		
7	pd_cal	Active high to power down VCO calibration; bit <7> = 0 for normal operation
6	muxout	Multiplexer control for ability to read byte 15; bit <6> = 1 for normal operation
5	pdcalc15	Active high to power down VCO ALC; bit <5> = 1 for normal operation
4	pload	Active high to load adjustment of VCO; bit <4> = 1 for normal operation
3	wide_1	Control for VCO ALC loop; bits <3:2> = 01 for normal operation
2	wide_2	
1	slew_1	Slew rate control of sub-integer N divider; bits <1:0> = 10 for normal operation
0	slew_0	

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Table 4.6 Register Byte Functions

Bit	Name	Function
BYTE 15		
7	comp_p	Synthesizer lock indication (read only): bits <7:6> = 01 locked, = 11 above window, = 00 below window, = 10 disallowed indicating error
6	comp_n	
5	rdacmsb_2	Reserved (read only)
4	rdacmsb_1	
3	rdacmsb_0	
2	rdacmux_0	
1	rdacmux_1	
0	rdacmux_2	

Table 5.1 540 MHz Channels

Channel	Divider	Band[1]	Byte 10	Byte 11
57.24	10101	001	11110001	01010011
57.78	10100	001	11110001	01000011
58.32	10011	010	11110001	00110101
58.86	10010	010	11110001	00100101
59.40	10001	011	11110001	00010111
59.94	10000	011	11110001	00000111
60.48	11111	100	11110001	11111001
61.02	00000	100	11110000	00001001
61.56	00001	101	11110000	00011011
62.10	00010	101	11110000	00101011
62.64	00011	110	11110000	00111101
63.18	00100	110	11110000	01001101
63.72	00101	111	11110000	01011111
64.26[2]	00110	111	11110000	01101111
64.80[2]	00111	111	11110000	01111111

Reference: 308.571 MHz

Note 1: Band setting typical, may change from module to module and temperature.

Note 2: Operation above 64 GHz not guaranteed over full operating temperature range.

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Table 5.1 500 MHz Channels

Channel	Divider	Band[1]	Byte 10	Byte 11
57.0	00001	000	11110000	00010001
57.5	00010	000	11110000	00100001
58.0	00011	001	11110000	00110011
58.5	00100	001	11110000	01000011
59.0	00101	010	11110000	01010101
59.5	00110	010	11110000	01100101
60.0	00111	011	11110000	01110111
60.5	01000	011	11110000	10000111
61.0	01001	100	11110000	10011001
61.5	01010	100	11110000	10101001
62.0	01011	101	11110000	10111011
62.5	01100	101	11110000	11001011
63.0	01101	110	11110000	11011101
63.5	01110	110	11110000	11101101
64.0	01111	111	11110000	11111111

Reference: 285.714 MHz

Note 1: Band setting typical, may change from module to module and temperature.

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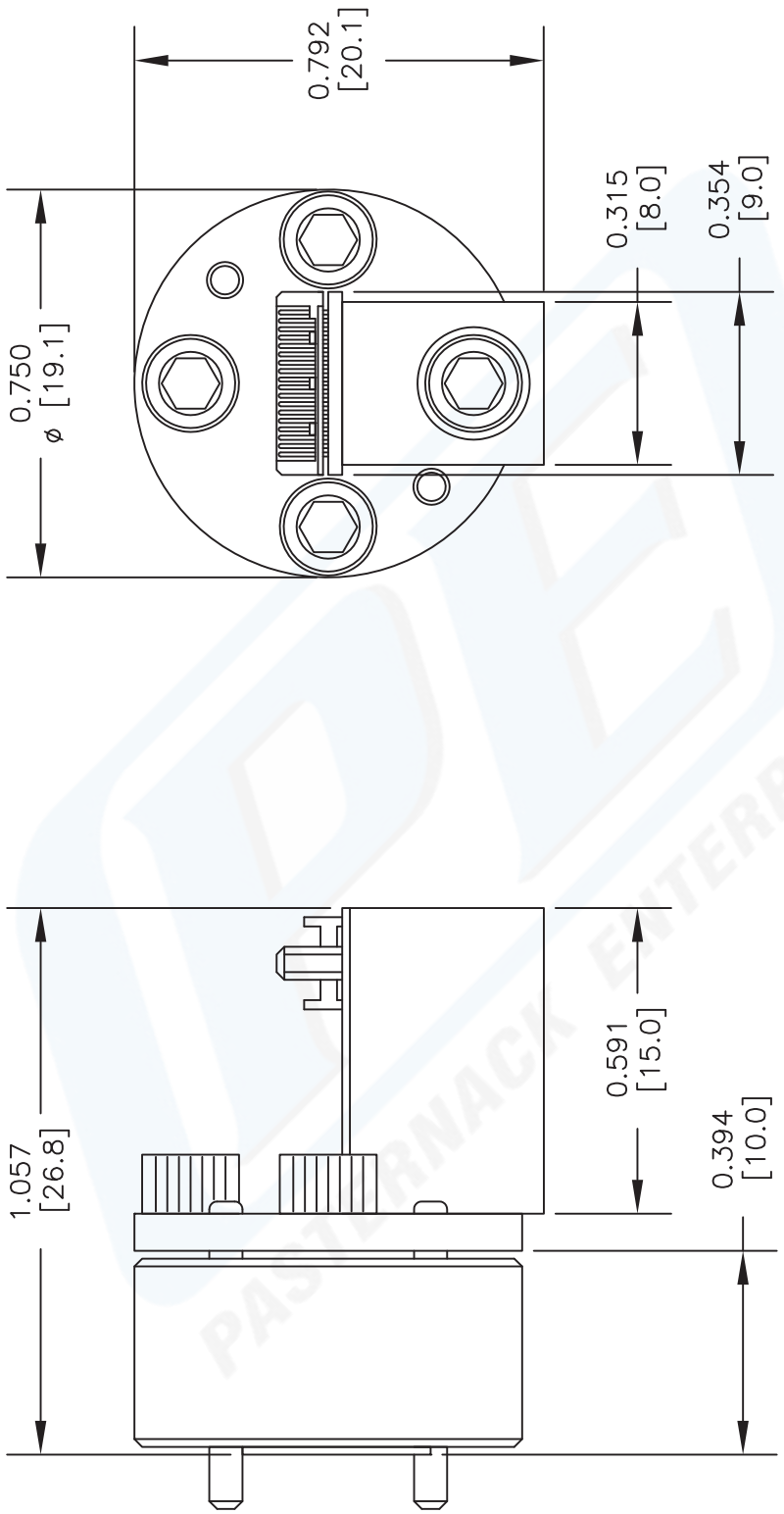
PEM002 CAD Drawing

Millimeter Wave Receiver Module Operating From 57 GHz To 64 GHz



NOTES:
1. UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE NOMINAL.
2. ALL SPECIFICATIONS ARE SUBJECT TO CHANGE WITHOUT NOTICE AT ANY TIME.
3. DIMENSIONS ARE IN INCHES [mm].
4. FITS MIL-C-17 AND EQUIVALENT CABLES.

CAD FILE	061813	SCALE N/A	SIZE A	2233

DWG TITLE **PEM002**

FSCM NO. 53919

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